Advancing GaN Electronics through Substrate Engineering and Integration

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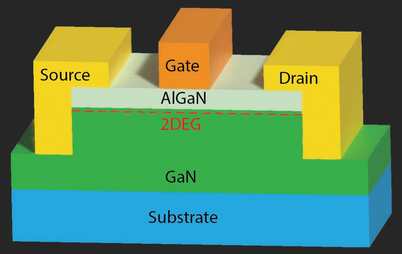
Substrate Selection

- GaN high electron mobility transistors **(HEMT)** offer higher performance for high-power and high-frequency applications.
- Free standing GaN is difficult and prohibitively expensive to grow, so heteroepitaxially grown layers are relied upon by industry.



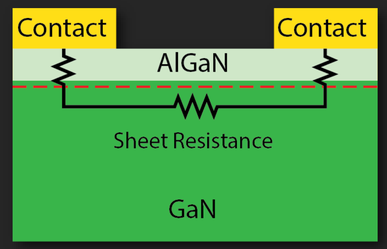
	Crystal Structure	Lattice Mismatch (%)	CTE Mismatch (%)
GaN	HCP	------	-----
Si	FCC	-16.5	55
SiC	HCP	3.5	30
Sapphire	HCP	16.8	-23

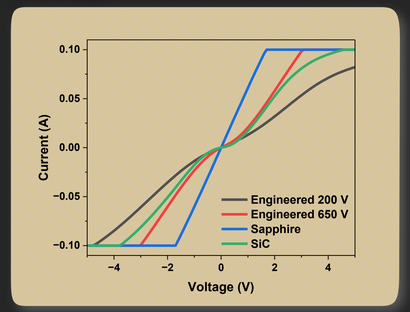
- While SiC offers the closest crystal properties and the highest thermal conductivity, it is an order of magnitude more expensive.
- Engineered substrate bridge the gap between cost, size, and performance.

Substrate Comparison

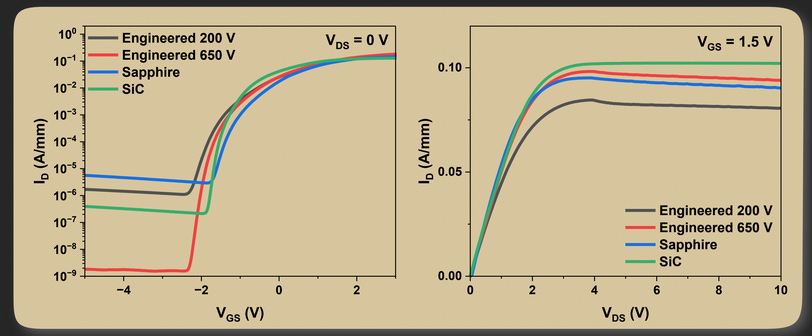
	Sheet Resistance (Ω/■)	Specific Contact Resistance ($\mu\Omega \cdot cm^2$)
QST 200 V (Engineered)	2630	120
QST 650 V (Engineered)	1630	212
MSE on Sapphire	802	71.9
Qorvo 09 on SiC	2440	1430

- Different substrates were tested to analyze performance.
- Circular transmission line measurements (CTLMs) were measured first.
- HEMT on Sapphire showed the lowest sheet and contact resistances.





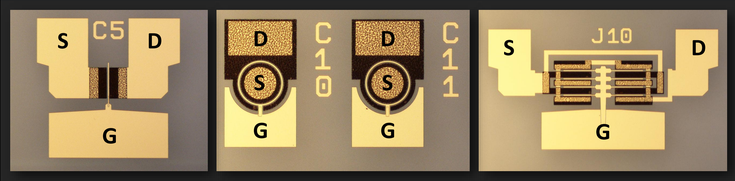
Device Comparison



	V_{TH} (V)	I_{ON}/I_{OFF}	R_{ON} (Ω/mm)
QST 200 V (Engineered)	-1.13	1.07×10^5	22.4
QST 650 V (Engineered)	-1.07	7.08×10^7	20.6
MSE on Sapphire	-0.99	2.49×10^4	18.0
Qorvo 09 on SiC	-1.06	1.47×10^5	17.8

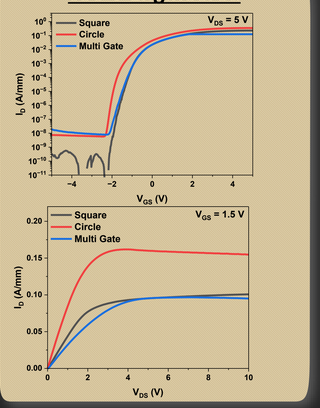
- While sapphire has low resistance, also has high leakage.
  - High defectivity.
- SiC has best overall performance and better thermal management.

Device Design

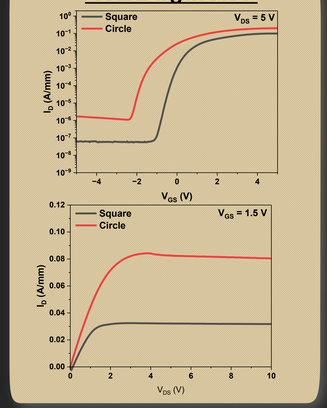


	Engineered 650 V			Engineered 200 V		
	V_{TH} (V)	I_{ON}/I_{OFF}	R_{ON} (Ω/mm)	V_{TH} (V)	I_{ON}/I_{OFF}	R_{ON} (Ω/mm)
Square	-0.762	4.04×10^8	35.4	-0.382	9.97×10^6	35.6
Circle	-1.07	7.08×10^7	20.6	-1.13	1.07×10^5	22.4
Multi-Gate	-0.82	$> 1.11 \times 10^7$	38.1			

650 V Engineered



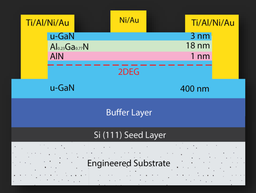
200 V Engineered

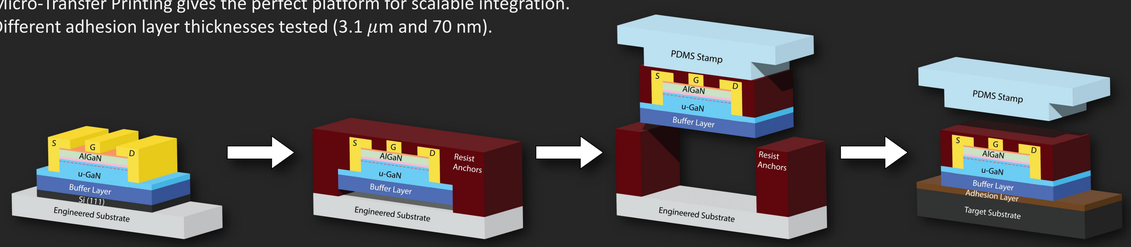


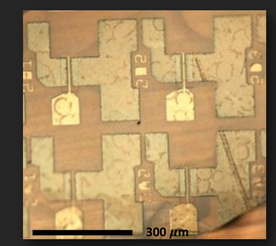
- Different geometries were tested to find the structure with the highest current densities.
- Circular devices consistently have the best performance.

Heterogenous Integration

- By releasing the device from the engineered substrate and transferring to a target substrate, we can get better performance.
- Micro-Transfer Printing gives the perfect platform for scalable integration.
- Different adhesion layer thicknesses tested (3.1 μm and 70 nm).



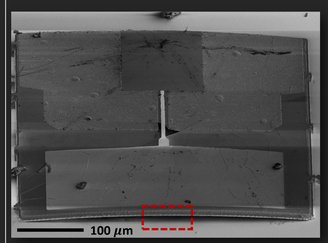


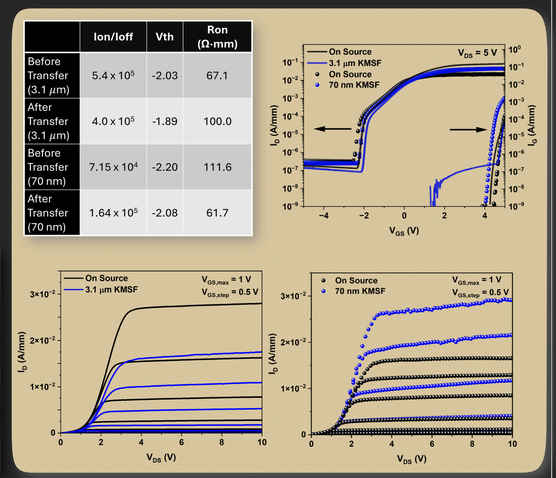


650 V Transfer

- High (>95%) success rate of the release and transfer was achieved to both adhesion layers.
- Minor change in device performance after transfer.
- Stress within the layers led to a 12 μm bend after transfer.

	Ion/Ioff	Vth	Ron (Ω·mm)
Before Transfer (3.1 μm)	5.4×10^5	-2.03	67.1
After Transfer (3.1 μm)	4.0×10^5	-1.89	100.0
Before Transfer (70 nm)	7.15×10^4	-2.20	111.6
After Transfer (70 nm)	1.64×10^5	-2.08	61.7

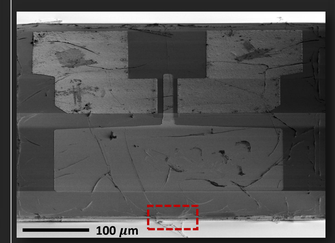


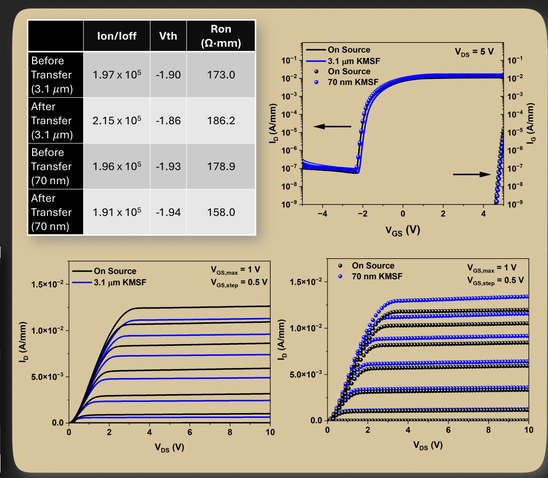


200 V Transfer

- High (>95%) success rate of the release and transfer was achieved to both adhesion layers.
- Lower stress within the system led to a flat device after transfer.
- Better reliability and minimal change in device performance after transfer.

	Ion/Ioff	Vth	Ron (Ω·mm)
Before Transfer (3.1 μm)	1.97×10^5	-1.90	173.0
After Transfer (3.1 μm)	2.15×10^5	-1.86	186.2
Before Transfer (70 nm)	1.96×10^5	-1.93	178.9
After Transfer (70 nm)	1.91×10^5	-1.94	158.0





Acknowledgements

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