3-D Full-Band Monte Carlo Simulation of Hot-Electron Energy Distributions in Gate-All-Around Si Nanowire MOSFETs

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***Abstract*— The energy distributions of electrons in gate-all-around (GAA) Si MOSFETs are analyzed using full-band 3-D Monte Carlo (MC) simulations. Excellent agreement is obtained with experimental current–voltage characteristics. For these 24-nm gate length devices, the electron distribution features a smeared energy peak with an extended tail. This extension of the tail results primarily from the Coulomb scattering within the channel. A fraction of electrons that enter the drain retains their energy, resulting in an out-of-equilibrium distribution in the drain region. The simulated density and average energy of the hot electrons correlate well with experimentally observed device degradation. We propose that the interaction of high-energy electrons with hydrogen-passivated phosphorus dopant complexes within the drain may provide an additional pathway for interface-trap formation in these devices.**

***Index Terms*— 3-D electron transport, Coulomb interactions, gate-all-around (GAA), hot electrons, Monte Carlo (MC), plasma scattering, radiation effects, reliability, Si technology, source depletion.**

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I. Introduction

HOT carrier effects (HCEs) in highly scaled devices are relevant at both high and low electric fields [1], [2]. HCEs in low-voltage, nanoscale devices are typically considered to be driven by multicarrier processes [3]. Long high-energy tails from electron–electron scattering (EES) influence these processes [4], [5], resulting in multiple activation energies for defect creation [6]. This behavior contrasts with simplified electric-field-based pictures of HCE that are commonly applied to larger devices.

Gate-all-around (GAA) devices are promising for next-generation technologies, offering excellent electrostatic control and reduced short-channel effects. While the reliability of planar field-effect transistors (FETs) and FinFET technologies has been extensively characterized, little is known about HCE in GAA topologies. Recently, Chasin *et al.* [7]–[9] performed an experimental investigation of reliability issues in GAA Si NW devices ($L_G = 24$ nm, channel diameter of 9 nm, and effective oxide thickness (EOT) = 0.85 nm). GAA devices were found to have similar bias-temperature instability to FinFETs. Threshold-voltage shifts, transconductance degradation, self-heating, and high-power dissipation remain major reliability concerns. These effects may reduce current drive, maximum operational frequency, and device lifetime. In addition, since the oxide surrounds the channel, power dissipation problems may be worse for GAA MOSFETs than for FinFETs. Hence, electron distributions and HCE are of significant interest for these devices.

In this article, we report 3-D full-band Monte Carlo (MC) simulations for a GAA Si nanowire (NW) MOSFET, solving the Boltzmann transport equation by incorporating various scattering processes. Scattering processes, such as intervalley, carrier-phonon, impact ionization, ionized-impurity, and carrier–carrier scattering [10]–[13], included in the present MC approach, are critical for a complete description of the high-energy tails [14]–[17]. Excellent agreement between the simulated and experimental current–voltage (I–V) characteristics is obtained.

The simulated electron energy distributions depend on the drain (V_{DS}) and overdrive ($V_{GS} - V_{Th}$) voltages. Some of the electrons have energies well above the ballistic peak due to impact ionization, localized momentum transfer, and carrier–carrier interactions. Trends in the simulated electron energy distributions match well with trends in experimental studies of device degradation reported in [7]. Our results suggest that the presence of a high concentration of energetic carriers in the drain may lead to the creation of interface traps via an additional pathway initiated by the release of hydrogen from P–H complexes in the drain.

II. 3-D Full-Band Ensemble Monte Carlo Transport Model for Hot Carriers

Lucky electron [18], [19], drift-diffusion [20]–[23], hydrodynamic [24], [25], and, more recently, virtual source [26]–[29] models have been used extensively to simulate electronic transport in Si devices. Often, these approaches use simplified energy and momentum relaxation times or averaged quantities, such as injection velocity, mean free path, and apparent (ballistic) mobility [28], which are useful but limited in analyzing high-energy transport effects [30], [31]. Using these simulation techniques, early predictions of device performance were optimistic for highly scaled devices [32], [33]. In contrast, only a sublinear improvement of the current and speed is achieved in practice. In extreme cases, electron velocities have declined with additional downscaling of transistor dimensions [34]–[36]. Overly optimistic predictions of earlier simulation techniques occur because they do not account for short-/long-range interactions [12], [37]–[39].

Long-range interactions enable electrons in the S/D regions to directly exchange energy with electrons in the channel through plasma oscillations. In sub-40-nm devices, plasma processes are more important than in larger devices [40] because of the proximity of the channel to the entire S/D regions. Due to this proximity, a significant fraction of the channel electrons exchanges momentum with electrons within the S/D regions [37]. This strong momentum transfer and associated enhancement of the hot-electron distribution can be reduced with lower doping levels within S/D regions [41]. However, reducing S/D doping to bypass plasma effects is often not plausible due to source starvation. Source starvation is a condition that occurs when there are not adequate numbers of carriers with a velocity component in the longitudinal direction; this is a known issue that restricts device scaling [37], [42].

Plasma interactions remain relevant even with metal gates and high-K materials used in modern technology. These increase the energy of plasma waves and weaken long-range scattering [12]. Moreover, short-range interactions modify the energy distribution and indirectly affect energy and momentum relaxation times [40], [43]. Thus, considering only long-range processes is not sufficient to simulate the energy distribution function.

The 2-D MC simulations by Fischetti and Laux [12] quantified the importance of treating short- and long-range carrier interactions and their nontrivial contributions to the resulting energy distributions and reliability. The combined effects of plasma and source starvation are articulated by Fischetti *et al.* [37], where static approximations (e.g., injection velocity) in virtual source models are shown to be inadequate. The virtual source region's potential adjacent to the source-channel junction is influenced by scattering events that occur throughout the channel. The resulting local potential fluctuations and changes in velocity are better captured using a physics-based simulation approach [37]. Uechi *et al.* [38], [39] treated both short- and long-range Coulomb interactions in 3-D and showed that potential fluctuations in a highly doped region ($> 1 \times 10^{20}$ cm^{-3}) may be as large as 0.20 eV and can be treated accurately using a semiclassical MC approach.

In this work, we use a high-fidelity code similar to Damocles, developed by Jin *et al.* [13], Fischetti [15], Frank *et al.* [43], and Fang *et al.* [44], [45], which solves Poisson's equation in 3-D to appropriately characterize momentum relaxation in all dimensions. The 2-D code has been validated extensively with experimental data [13], [14], [41]. The device is simulated using a finite-difference tensor mesh. Electrons in the Si NW are modeled as MC particles with effective electron charge weight smaller than one; holes are included in a constant quasi-Fermi level (zero current) approximation. Simulations include scattering with acoustic phonons, optical phonons, impact ionization, and short-/long-range interactions (plasma, potential fluctuations, and carrier–carrier) with full electronic energy bands [31].

EES is treated using the method described in [11, Appendix A], [12, Appendix C1], and [46]. Short-range interactions of hot carriers in the channel with cold carriers of the drain are dynamically screened. Long-range interactions (plasma oscillations) are semiclassically treated using a self-consistent solution of Poisson's equation. Mesh spacing is set at 2.8 Å, as found to optimally represent the dependence of the Landau damping on electron concentration [41]. Tradeoffs are necessary due to conflicting requirements of mesh spacing and charge weight [47]. To reduce the complexity of the 3-D inhomogeneous device simulations, plasma oscillations are treated as particles carrying 0.1 electron charge to achieve the necessary computational statistics [12], [47].

A Poisson time step of 0.2 fs is used for all computations. The Gilat–Raubenheimer algorithm [48] is used to calculate densities of states for the conduction and valence bands. Carrier-phonon scattering rates are computed using the deformation potentials of [41]. The impact-ionization model [49], [50] has been obtained by fitting a Keldysh-like energy dependence to the ionization rate calculated using the empirical-pseudopotential energy band structure and calibrated to the X-ray photoelectron spectroscopy and carrier separation

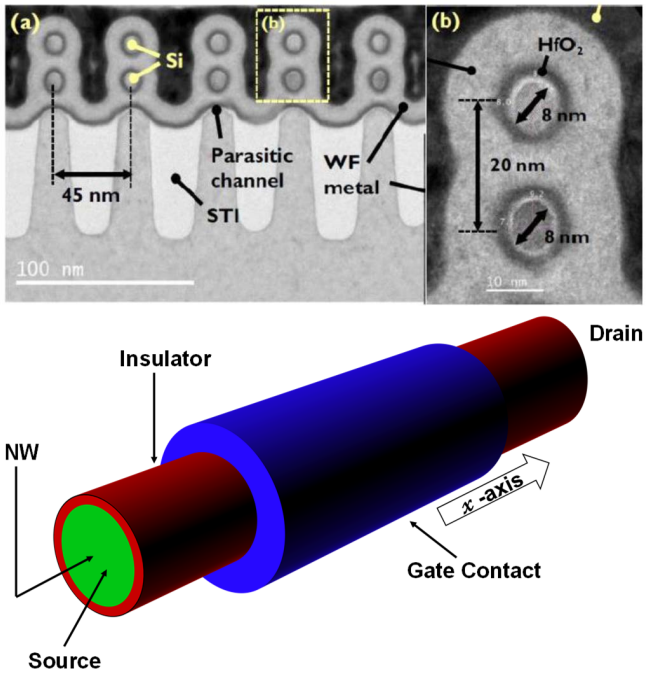

Fig. 1. TEM images of a GAA Si nMOSFET from imec [53] depicting (a) NW array and (b) single NW vertical stack. WF metal represents the work-function metal used for the gate electrode. (c) Schematic of the simplified device used for simulation (not drawn to scale). The insulating oxide in the S/D access region and gate contact extends radially outward until the end of the tensor mesh (not shown).

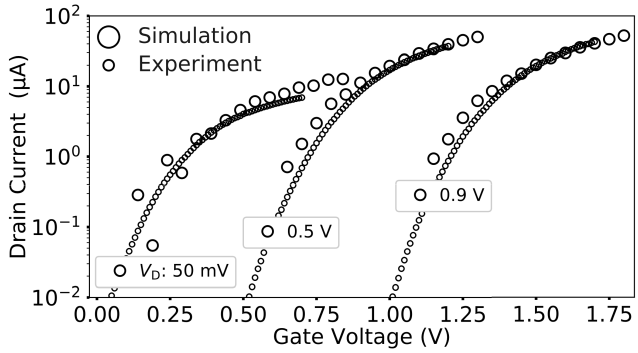

Fig. 2. Experimental and simulated gate control at 50-mV, 0.5-V, and 0.9-V drain bias. Curves are shifted along the x-axis by −0.5, 0.0, and 0.5 V, respectively. The experimental drain current is divided by 2 to match the simulated I–V characteristics of the single NW structure depicted schematically in Fig. 1(c).

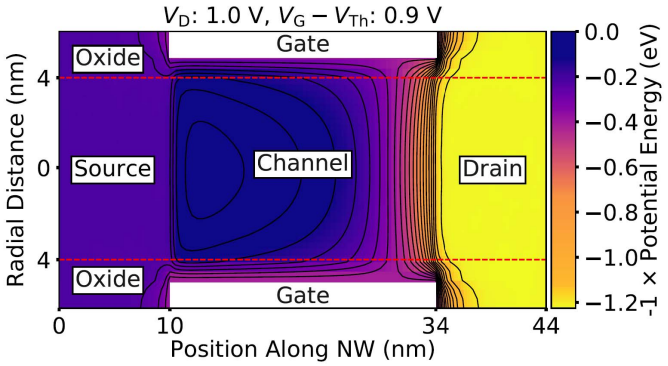

Fig. 3. Electron potential energy along the x-direction of the cylinder in Fig. 1(c), illustrated with a color map. The density of the equipotential lines reflects the magnitude of the electric field. Metallurgical junction boundaries are at $x = 10$ and 34 nm. The red dashed lines separate the oxide and semiconductor regions of the device. The aspect ratio is different from actual device dimensions for clarity.

experimental data [51]. Carrier-phonon scattering and impact ionization models have been validated in Si with experiments up to electron energy of 7.2 eV [44]. Ionized-impurity scattering is treated via the Conwell–Weisskopf model [52]. The oxide is treated as an ideal insulator, with no carriers present. Electron collisions at the oxide interface are specular and conserve momentum. The relative dielectric constant is adjusted to produce an EOT of 0.85 nm, consistent with [53].

Effects of quantum confinement were found to be negligible in previous work on devices of similar or smaller dimensions and were not included in the simulations [54], [55]. For example, calculations of the band structure of circular-cross section Si NWs using empirical pseudopotentials show that the lowest-energy subbands are spaced by about 0.2 eV for a diameter of 2.5 nm [54]. Rescaling by the square of the ratios of the respective diameters, this value drops to ∼20 meV for the NWs of this work. Moreover, MC simulations of rectangular cross section NWs by Donetti *et al.* [55] solved Poisson's equation in 3-D and the Schrödinger equation in 2-D and treated transport as ballistic in 1-D. For NW diameters larger than 4 nm, they find that, except for a V_{Th}-shift, the current is not affected by quantum effects in Si NWs. Hence, our simulations did not include quantum confinement. The source-to-drain tunneling is also not considered since it is not important for devices with a gate length greater than ∼10 nm [56]–[58].

III. Carrier Transport in a Si Nanowire MOSFET

Fig. 1(a) and (b) shows n-channel GAA MOSFETs fabricated at imec [53] (L_G = 24 nm, channel diameter 8 nm, EOT = 0.85 nm, S/D dopant density = 5×10^{20} cm^{-3}, and channel acceptor density = 1×10^{18} cm^{-3}). A single NW similar to Fig. 1(c) is considered in the simulations [53], but the results are also relevant to vertically stacked NWs in the absence of significant contact resistance and other parasitic effects, which are expected to be small in optimized processes of practical interest. Instead of crudely representing an NW with a square cross section [55], we closely approximated the circular shape via a tensor mesh with mesh-node density (defined by the constraints on grid-spacing to accurately account for long-range interaction) of 12.5 nm^{-2}. This approximation is acceptable since the periodic fluctuation (0–0.14 nm) of the radius of the simulated NW is smaller than that of the physical device due to process variations [7].

Fig. 2 compares I–V curves for experimental and simulation results. The simulated characteristics agree well with experimental measurements over five orders of magnitude variation in current. The work function of the metal gate is adjusted in simulations to match the gate control of the physical device.

For a device operating in deep saturation (V_{DS} = 1 V), the densest equipotential lines overlying the potential plot in Fig. 3 correspond to a localized field peak near the metallurgical drain junction at x = 34 nm.

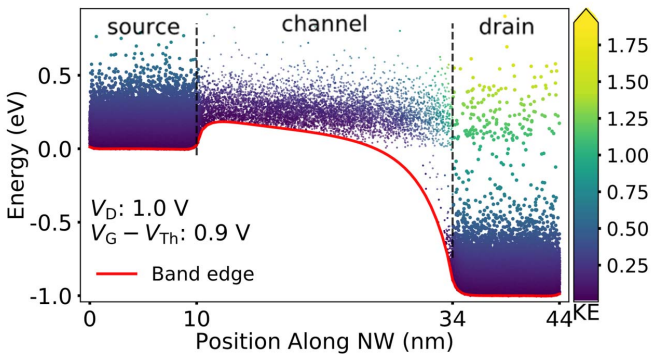

Fig. 4. Carrier KE distribution above the conduction-band edge along the *x*-direction of the device. The conduction-band edge is averaged over the cross section of the channel. Statistical carrier enhancement within the dashed vertical lines ensures adequate sampling of interactions in an otherwise sparsely populated region. The KE of the carriers is represented by both particle color and the distance above the conduction band.

Conversely, the electron energies that are plotted versus position along the channel in Fig. 4 display a dispersed hot carrier distribution similar to earlier MC simulations of a 30-nm-long double-gate Si MOSFET [43]. In this work, we will refer to carriers with energies higher than 0.5 eV as "hot" [3], [5], [7]. Due to the limited volume of the drain access region (34 nm $<\times<$ 44 nm), approximately 10% of the hot carriers in the distribution in Fig. 4 do not lose energy in the drain. Instead, they leave—still hot—the simulated region via the metallurgical contact to the drain. This is understandable because the drain dimension (∼10 nm) is smaller than the mean free path for collisions of electrons in silicon.

IV. Spatial and Energy Distribution of Hot Electrons

In designing reliable devices, it is important to understand the sensitivity of the carrier energy to the drain and gate bias [4]–[6], [59]. Fig. 5 shows the kinetic energy (KE) distribution of the electrons as a function of drain bias V_{DS} for a gate-voltage overdrive $V_{Ov} = V_{GS}-V_{Th} = 1.3$ V. The solid and dotted curves correspond to simulation results obtained with and without EES, respectively.

Calculated electron-energy distributions are obtained by considering carriers in a volume around the metallurgical drain junction, 32 nm $<\times<$ 36 nm. The KE distribution in Fig. 5(a) displays a cold carrier peak at approximately 0.15 eV, followed by a dispersed hot-carrier population due to field-driven acceleration of electrons as they transport from source to drain. As shown in Fig. 4, the cold-carrier peak features a higher electron effective temperature due to degeneracy (5×10^{20} cm^{-3}) heating and long-range plasma interactions [12], [37], [60]. In addition to other Coulomb interactions [40], the tail of the cold-carrier distribution is enhanced due to EES, as evidenced by the close differences among the solid and dotted lines.

In addition to the expected heating of the carriers with increasing V_{DS}, the hot-carrier population in Fig. 5(a) shows a broad secondary peak at energy given roughly by $qV_{DS}+E_{\{Fs\}}$,

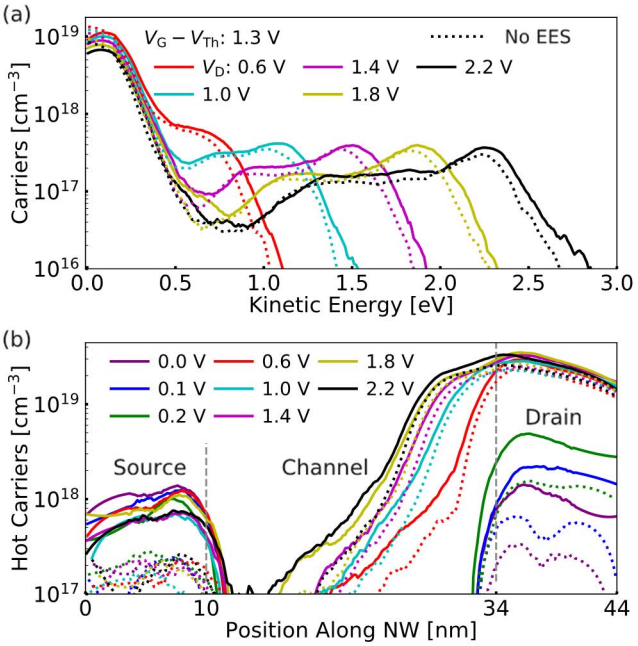

Fig. 5. Energy distribution of electrons for several drain biases at $V_{GS}-V_{Th} = 1.3$ V. (a) Electron-energy histogram within 2 nm in each direction of the metallurgical drain junction. (b) Density of electrons above 0.5 eV in the NW. The dotted curves show results without including EES.

where $E_{\{Fs\}}$ is the Fermi level of the source contact, approximately at 0.15 eV. Simple models of hot-electron degradation typically assume that no electron exceeds the Si bandgap energy (1.12 eV) when the supply voltage (V_{DD}) is lower than 1.12 V [7]. In contrast, at $V_{DS} = 1.0$ V, the hot electron distribution has a broad peak above 1.1 V and a tail that extends past 1.5 eV. Higher V_D values lead to similarly shaped distributions that extend to even higher energies and exhibit longer tails.

The smearing of the high energy peak indicates that electron transport is not ballistic, and electrons are strongly scattered by phonons, short- and long-range Coulomb processes, and so on. The shape of the KE distribution is similar to previous studies that include these processes [12], [40], [41]. EES contributes significantly to the hot-carrier population and extends the tail of the distribution [61].

For a constant overdrive voltage, Fig. 5(b) shows that the hot-carrier density at or near the drain junction increases up to deep saturation, $V_{DS} = 0.6$ V. However, the full-width at half-maximum (FWHM) continues to increase at high drain biases. The large FWHM affirms that a significant number of hot electrons do not thermalize upon reaching the 10-nm drain region. The effects of plasma interactions and potential fluctuations between the channel and S/D are particularly visible at $V_{DS} = 0$ V since the external field that accelerates the electrons along the longitudinal direction is absent. As shown in Fig. 5(c), a significant density of hot electrons at $V_{DS} \geq 0.2$ V indicates that carriers energetic enough to cause damage by collective processes (e.g., multicarrier, multiple activation energies, and trapped states) are generated at nominal bias conditions in this technology. Comparisons of the solid and dotted curves show that EES strongly increases the

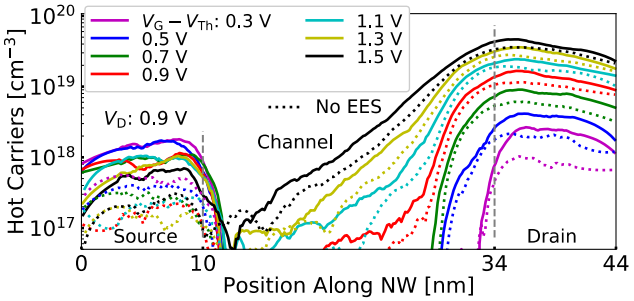

Fig. 6. Density of electrons above 0.5 eV in the NW for several overdrive biases at $V_{DS} = 0.9$ V. Dashed lines show the hot-electron distribution without EES.

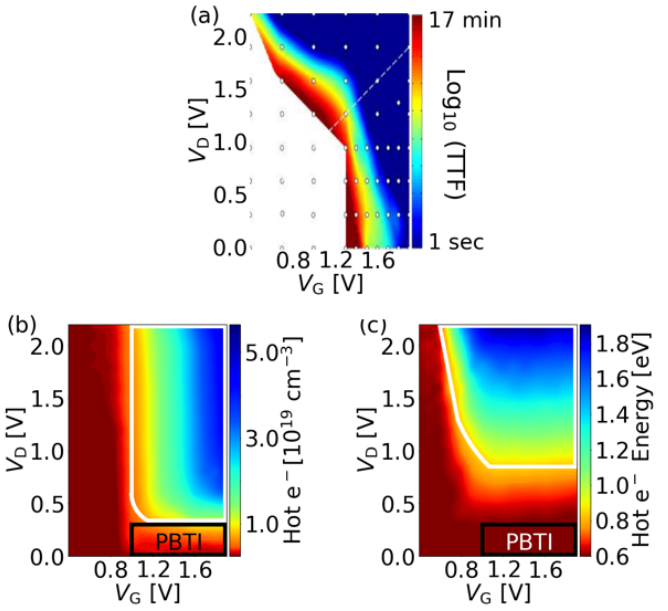

Fig. 7. (a) Experimentally derived time-to-failure (TTF) maps of the GAA device, adapted from Chasin *et al*. [7]. (b) Simulated density of hot carriers in a small volume near metallurgical junction ∼ within ±2 nm in the *x*-direction. (c) Simulated average KE of these hot electrons. Only the electrons with energy higher than 0.5 eV are considered for subplots (b) and (c). Scales of the color bars in (a) are logarithmic, and those in (b) and (c) are linear.

hot-electron population in the S/D. In addition, the hot-carrier population in the channel is broadened by EES, especially at higher biases. Moreover, comparisons of hot-electron densities in the source region at low and high drain biases indicate that source starvation is not a concern at the doping level (5×10^{20} cm^{-3}) of this work.

For the worst case HCE in ultrascaled devices, both the maximum energy and the carrier flux impinging on the interface play crucial roles [19], [62], [63]. The number of electrons in the channel of an ultrascaled transistor depends on both V_{DS} and V_{GS} since the electrostatic coupling between the terminals becomes stronger as the device shrinks. Furthermore, the small S/D volume limits the maximum electron current since the reservoir cannot keep up with carrier flow in the channel. Fig. 6 shows that the magnitude and FWHM of the hot-electron density depend strongly on the gate-overdrive voltages. Strong enhancement of the hot-carrier population throughout the device by EES is again observed for the curves in Fig. 6. A significant hot-electron density is observed at $V_{Ov} = 0.3$ V, suggesting that a value of $V_{DS} = 0.9$ V can introduce enough energetic electrons to accelerate the device degradation even when the applied V_{Ov} is small. The damage caused by hot-electron processes becomes more significant with increasing V_{Ov} due to the subsequent increase of the electric field toward the interface. For the biasing conditions considered here, simulations of bipolar carrier transport show that the hot (>1 eV) hole density in these structures is at least six orders of magnitude smaller than the density of hot electrons. Moreover, the electric field is not sufficiently strong to accelerate holes to high enough kinetic energies to cause significant degradation [7], [15], [64]–[66].

V. Comparison With Experimental Results

Recently, Chasin *et al.* [7] have reported experimentally derived time-to-failure data (TTF) of the GAA device examined here. We show an adapted version of their figure in Fig. 7(a). The dependence of the failure rate on the energy and density of hot electrons is highly complex and highly nonlinear. Hot-carrier-induced degradation is driven by both the maximum energy and the density (flux) of the hot electrons [61], [67]. Within the framework of the theory of the inelastic scattering of hot electrons at defects [68], [69], which can lead to their activation, the pertinent cross section depends on both the maximum energy that can be dissipated in a scattering event and the density of hot carriers that can deliver the required amounts of energy.

In Fig. 7(b) and (c), we show the density and mean energy of the hot electrons, respectively. We focus first on the areas bounded by white lines in Fig. 7(b) and (c). In this regime, both the drain and gate voltages are relatively high, and hot carriers are abundant. In similar voltage ranges in Fig. 7(a), device lifetimes are greatly reduced. The overall similarity of our simulation results and data in Fig. 7(a) strongly suggests that HCEs play a role in causing device failure in these voltage ranges. When the drain voltage is lower, HCE effects become negligible, and other mechanisms, such as positive bias-temperature instability (PBTI), limit device lifetime [7], [70], [71].

We now consider how hot electrons near and/or within the highly doped drain may lead to hot-carrier effects. One mechanism that has been considered extensively in the literature is multivibrational excitation (MVE) [3]–[6], [8], [72], [73]. The energy required to break a Si–H bond is ∼2.6 eV [74]–[76]. The MVE model presumes that multiple scattering events at a hydrogen-passivated dangling silicon bond (Si–H) at the SiO_2 interface can provide enough energy to liberate the passivating hydrogen atom, leaving behind an interface trap [3]–[6].

The presence of a high density of hot electrons in the highly doped drain demonstrated here suggests that the second potential mechanism for hot-electron-induced interface-trap creation is also likely in these devices. The drains of these devices are highly doped with phosphorus [75], [77]. The injection of hydrogen in devices during processing, which is

needed to passivate defects, such as interfacial Si dangling bonds, inevitably passivates a significant fraction of dopant atoms as well [76]–[80]. The energy required to break a P–H bond associated with a passivated dopant complex in the drain is ∼1.3 eV [81]. Once a hydrogen atom is liberated from a dopant atom, it can diffuse rapidly until it either encounters another H atom and dimerizes or encounters an energetically favorable reaction site. The energy for a diffusing hydrogen atom to react with a Si–H bond, leading to interface-trap creation, is typically of order ∼0.3–0.4 eV [76], [80], [81]. Thus, the presence of a high concentration of carriers in the drain with energies above ∼1.3 eV may lead to the release of atomic hydrogen, diffusion of a percentage of the liberated atomic hydrogen to the nearby channel, and its subsequent reaction with Si–H bonds to create interface traps [80]–[86]. In nanoscale devices, the presence of even a few interface traps near the drain junction can greatly degrade device performance [6], [7], [10], [11], leading to a significant reduction in lifetime.

Similar field- and/or carrier-induced release of hydrogen from passivated dopant complexes in the Si substrate has been proposed as a rate-limiting step in negative bias-temperature instability (NBTI) in pMOS devices [80], [82]. For pMOS NBTI, the barrier for hydrogen release from dopant atoms is reduced by the high densities of holes in the substrate [82]. For nMOS HCE in these nanoscale devices, the presence of a high density of electrons with energies within the drain can be the initiating step in the process. The energetics of trap creation are, otherwise, similar after the hydrogen is released [76], [80]–[86]. In contrast to NBTI, the PBTI process that is expected to dominate device degradation at the high oxide electric fields present in these devices under the conditions of the experiments in Fig. 7(a) does not depend on hydrogen release and/or reaction. Instead, the PBTI in these devices is typically a result of electron tunneling into border traps, a process with very different energetics and kinetics. Whether HCE or PBTI is the rate-limiting process in device operation is determined by biasing levels and fractions of lifetime during which the device is conducting versus the fraction of time during which the device is turned off. For cases in which HCE dominates, calculations similar to those shown in this work can be applied to assist in lifetime estimation. For cases in which PBTI effects dominate, alternative models have been developed and must be applied [7], [71], [87].

Due to the significant reduction in bond-breaking energies, hydrogen release from a P–H complex (∼1.3 eV barrier [81]) in the drain can occur much more easily as the result of a single hot-carrier interaction than hydrogen release from a Si–H complex (∼2.6 eV barrier [74], [76], [77]). Which of these mechanisms dominates for a particular device depends on a number of factors, including: 1) the channel current density; 2) densities of electrons within the drain with energies greater than ∼1.3 eV; 3) relative densities of Si–H complexes along with the channel interface and P–H complexes within the drain; 4) the respective interaction cross sections between hot electrons and Si–H complexes at the Si/SiO_2 interface and P–H complexes within the drain; and 5) probabilities that a hydrogen atom (charged or neutral) dimerizes with another hydrogen atom or forms another complex before reaching the channel/SiO_2 interface.

It is beyond the scope of this work to develop a quantitative model of hot-carrier degradation initiated by P–H bond breaking due to hot carrier interactions within the drain. Regarding the development of such a future model, we note the following.

1) The channel current density can be determined experimentally.
2) The calculation methods of this work provide the necessary information about carrier energies.
3) Si–H and P–H densities and spatial distributions depend on the device processing and are generally not well known. Hence, at least initially, these would need to be treated as adjustable parameters.
4) Interaction cross sections for channel carriers and Si–H complexes have been calculated in MVE models (MVE) [3]–[6], [8], [72], [73], [88], but interaction cross sections with P–H complexes are not well known at the energies relevant to this work.
5) The diffusion and reactions of hydrogen within Si MOS devices have been studied in great detail for more than 40 years, and diffusion barriers and rates for hydrogen transport and reactions have been calculated for multiple species under a wide range of experimental conditions [4], [6], [76], [78], [79], [87]–[91].

We, therefore, expect that significant insight into reliability-limiting mechanisms for nanoscale devices could be obtained by evaluating the relative importance of hydrogen release from dopant complexes in hot-carrier-induced degradation in MOS devices.

VI. Conclusion

A comprehensive semiclassical model is used to investigate the electronic energy transport properties of a GAA Si NW MOSFET. Simulation results show that plasma effects and electron degeneracy elevate the energy of the electrons in the device in conjunction with other scattering mechanisms. Not all hot-electrons lose their energy after crossing the drain depletion region; instead, some move quasi-ballistically in the drain. The hot-carrier reliability of the GAA transistor is investigated by comparing experimental TTF to the simulated density and average energy of the hot carriers. We find that the average energy and density of hot-electrons correlate well with the measured TTF in ranges of operation for which both drain and gate voltages are applied for significant fractions of device lifetime. It is proposed that the release of hydrogen from passivated phosphorus dopant complexes in the drain and the subsequent reaction of diffusing atomic hydrogen with passivated silicon dangling bonds at the Si/SiO_2 interface may contribute significantly to hot-carrier-induced degradation in these nanoscale devices. When devices are primarily biased statically, other failure mechanisms, such as PBTI dominate, and different models must be applied.

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